AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-20. (Canceled)

21. (New) A cache control system connectable to a remote memory, the cache control system comprising:

a micro-controller for executing micro-controller data;

a buffer manager for arbitrating access to the remote memory;

a micro-controller cache system coupled to the micro-controller and the buffer manager for fetching and caching micro-controller data stored in the remote memory via the buffer manager for access by the micro-controller; and

a cache demand circuit coupled to the micro-controller and the micro-controller cache system for receiving an address in the remote memory from the micro-controller and transmitting the address to the micro-controller cache system;

wherein the micro-controller cache system is responsive to the transmitted address to fetch micro-controller executable data stored at the transmitted address before the micro-controller requests execution of the micro-controller executable data.

22. (New) The cache control system of Claim 21, wherein the cache demand circuit is further responsive to a memory access signal to transmit the address to the micro-controller cache system.

23. (New) The cache control system of Claim 22, wherein the cache demand circuit receives the memory access signal from the micro-controller.

24. (New) The cache control system of Claim 23, wherein the memory access signal comprises a write signal received from the micro-controller.

25. (New) The cache control system of Claim 22, further comprising an interrupt circuit for interrupting the micro-controller based on a transmitted interrupt signal.

26. (New) The cache control system of Claim 25, wherein the memory access signal comprises the transmitted interrupt signal.

27. (New) The cache control system of Claim 26, wherein the micro-controller executable data fetched by the micro-controller cache system is executed by the micro-controller during a micro-controller interrupt service routine.

28. (New) The cache control system of Claim 22, wherein the cache demand circuit receives the address from the micro-controller before the memory access signal.

29. (New) The cache control system of Claim 22, wherein the cache demand circuit is operable to store the address received from the micro-controller.

30. (New) The cache control system of Claim 22, wherein the cache demand circuit is operable to transmit the memory access signal to the micro-controller cache system.

31. (New) The cache control system of Claim 22, wherein the memory access signal comprises a servo-interrupt signal.

32. (New) The cache control system of Claim 22, wherein the memory access signal comprises a host-interrupt signal.

33. (New) The cache control system of Claim 21, wherein the buffer manager is in communication with a plurality of disk drive control system clients, including at least one

of a disk subsystem, an error correction code subsystem, and a host interface subsystem.

34. (New) A method for caching micro-controller data in a cache control system comprising a micro-controller, a buffer manager coupled to a remote memory, a micro-controller cache system coupled to the micro-controller and the buffer manager, and a cache demand circuit coupled to the micro-controller and the micro-controller cache system, the method comprising:

receiving at the cache demand circuit an address in the remote memory from the micro-controller;

transmitting the address from the cache demand circuit to the micro-controller cache system;

fetching micro-controller executable data stored at the address via the buffer manager; and

caching the micro-controller executable data stored at the address in the micro-controller cache system before the micro-controller requests execution of the micro-controller executable data.

35. (New) The method of Claim 34, further comprising receiving at the cache demand circuit a memory access signal, and wherein the step of transmitting the address from the cache demand circuit to the micro-controller cache system is taken upon receipt of the memory access signal.

36. (New) The method of Claim 35, further comprising transmitting the memory access signal from the micro-controller to the cache demand circuit.

37. (New) The method of Claim 35, wherein the memory access signal comprises a write signal.

38. (New) The method of Claim 35, wherein the memory access signal comprises an interrupt signal.

39. (New) The method of Claim 38, further comprising executing the micro-controller executable data stored at the address during a micro-controller interrupt service routine.

40. (New) The method of Claim 35, wherein the step of receiving the address occurs before the step of receiving the memory access signal.

41. (New) The method of Claim 35, further comprising storing the address in the cache demand circuit.

42. (New) The method of Claim 35, further comprising transmitting the memory access signal from the cache demand circuit to the micro-controller cache system.

43. (New) The method of Claim 35, wherein the memory access signal comprises a servo-interrupt signal.

44. (New) The method of Claim 35, wherein the memory access signal comprises a host-interrupt signal.

SUMMARY OF INTERVIEW

Applicant wishes to thank Examiner Ko for the interview conducted on May 3, 2006. The following summarizes the substance of the interview, in accordance with the guidelines provided by MPEP 713.04.

(A) No exhibit was shown, and no demonstration was conducted.

(B) Claim 1 was discussed in the context of a potential amendment.

(C) The teachings of Grimsrud *et al.* (U.S. Patent No. 7,000,077) were primarily discussed.

(D) Proposed amendments to Claim 1 were discussed. New Claim 21 is the result of those discussions.

(E) The general thrust of Applicant's arguments presented at the interview was that Grimsrud does not teach or suggest the cache demand circuit as originally claimed. The Examiner indicated that amendments to the claim should be made to clarify the differences between the claimed cache demand circuit and the teaching in Grimsrud.